

Abstract of the Disclosure

There is provided a Delay Locked Loop (DLL) including a duty cycle correction circuit capable of controlling a duty error, when the duty error is generated in the DLL. The duty cycle correction circuit controls amounts of electric charges accumulated in storage units, in response to switching control signals received from the external, and outputs duty rate control signals each corresponding to a difference between the amounts of electric charges accumulated in the storage units. Therefore, the DLL including the duty cycle correction circuit can correct a duty cycle of a reference clock signal, in response to the duty rate control signals, and can output a reference clock signal with a duty cycle of 50%.

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